Advisory Action Before the Filing of an Appeal Brief

Application No.	Applicant(s)	
10/799,375	SINDAGI ET AL.	
Examiner	Art Unit	
JESSE R. MOLL	2181	

	DECOE IV. WIGEE	2101
The MAILING DATE of this communication appe	ears on the cover sheet with the	correspondence address
THE REPLY FILED <u>26 November 2007</u> FAILS TO PLACE THIS	S APPLICATION IN CONDITION F	FOR ALLOWANCE.
1. The reply was filed after a final rejection, but prior to or on application, applicant must timely file one of the following application in condition for allowance; (2) a Notice of Application (RCE) in compliance with 37 C periods:	replies: (1) an amendment, affidav eal (with appeal fee) in compliance	it, or other evidence, which places the with 37 CFR 41.31; or (3) a Request
a) The period for reply expiresmonths from the mailing		
b) The period for reply expires on: (1) the mailing date of this A no event, however, will the statutory period for reply expire I Examiner Note: If box 1 is checked, check either box (a) or MONTHS OF THE FINAL DELECTION (See MEED 700 077).	ater than SIX MONTHS from the mailin (b). ONLY CHECK BOX (b) WHEN THE	g date of the final rejection.
MONTHS OF THE FINAL REJECTION. See MPEP 706.07 (Extensions of time may be obtained under 37 CFR 1.136(a). The date have been filed is the date for purposes of determining the period of ex under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the set forth in (b) above, if checked. Any reply received by the Office later may reduce any earned patent term adjustment. See 37 CFR 1.704(b) NOTICE OF APPEAL	on which the petition under 37 CFR 1.1 tension and the corresponding amount shortened statutory period for reply origet than three months after the mailing da	of the fee. The appropriate extension fee inally set in the final Office action; or (2) as
 2. ☐ The Notice of Appeal was filed on A brief in comp	pliance with 37 CFR 41.37 must be	filed within two months of the date of
filing the Notice of Appeal (37 CFR 41.37(a)), or any exte Notice of Appeal has been filed, any reply must be filed w AMENDMENTS	nsion thereof (37 CFR 41.37(e)), to	avoid dismissal of the appeal. Since a
 The proposed amendment(s) filed after a final rejection, (a) They raise new issues that would require further co (b) They raise the issue of new matter (see NOTE below) 	nsideration and/or search (see NO	
(c) They are not deemed to place the application in bet appeal; and/or	tter form for appeal by materially re	
(d) They present additional claims without canceling a NOTE: (See 37 CFR 1.116 and 41.33(a)).		
4. The amendments are not in compliance with 37 CFR 1.1.		empliant Amendment (PTOL-324).
5. Applicant's reply has overcome the following rejection(s)		timely filed amondment concelling the
 Newly proposed or amended claim(s) would be al non-allowable claim(s). For purposes of appeal, the proposed amendment(s): a) 		
how the new or amended claims would be rejected is provided that the status of the claim(s) is (or will be) as follows: Claim(s) allowed: Claim(s) objected to: Claim(s) rejected: Claim(s) withdrawn from consideration:		ii be entered and an explanation of
AFFIDAVIT OR OTHER EVIDENCE		
 The affidavit or other evidence filed after a final action, bu because applicant failed to provide a showing of good and was not earlier presented. See 37 CFR 1.116(e). 		
 The affidavit or other evidence filed after the date of filing entered because the affidavit or other evidence failed to o showing a good and sufficient reasons why it is necessary 	overcome <u>all</u> rejections under appea	al and/or appellant fails to provide a
10. ☐ The affidavit or other evidence is entered. An explanatio REQUEST FOR RECONSIDERATION/OTHER	n of the status of the claims after e	ntry is below or attached.
 The request for reconsideration has been considered bu <u>See Continuation Sheet.</u> 	it does NOT place the application in	n condition for allowance because:
12. ☐ Note the attached Information <i>Disclosure Statement</i>(s).13. ☐ Other:	(PTO/SB/08) Paper No(s)	
/Alford W. Kindred/ Supervisory Patent Examiner, Art Unit 2163		
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Continuation of 11. does NOT place the application in condition for allowance because: Regarding the arguments directed to Kling not teaching data being unavailable, Inherently, data is not available before it is created. When a register is to be written by an instruction, the data is clearly not available before it the instruction completes and the data is written. The data is inherently made available when the instruction is written because the data now exists in the register. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., not stalling instructions,) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Regarding page 11, it is true that an instruction can write to a register which is used as an input. Applicant's argument is flawed because the instruction becomes unavailable for every instruction after that instruction. If the instruction after the instruction writing to a register tries to read that register, it is unavailable until the previous instruction executes. The input will read different data than the output. Any subsequent instruction will still inherently be blocked and the register will be unavailable until the instruction finishes. Therefore, as stated in the last office action, it is inherent that a write will cause a register to become unavailable (unless the processor is not pipelined which is clearly not the case here since scoreboarding is useless without a pipeline). Applicant states that the instruction "SUB .D1 A2.I.A2 ... does not make the register unavailable as an input operand or as a predicate". This however is incorrect because the register is unavailable for each instruction after that instruction until it is executed. If for instance, the next instruction were to reference A2, it would be unable to execute until the data became available. Claim 1 states "operating at a reduced power state... if said predicate register has said second state... and said corresponding scoreboard bit has said second state..." As stated in the office action, the combination would enter a reduced power state if the scoreboard bit had said second state. It does not matter the status of the predicate register and would enter a reduced power state "if said predicate register has said second state" or if said predicate register does not have said second state, clearly falling within the limitations of the claim. Regarding operating at normal full power operation during execution phase, the following execution phase is the phase in which nothing is executed because of the stall not the phase after the stall. Regarding when decisions are made, Examiner suggests clarifying the language to limit the claim in the way describe if that is what is desired. Currently, the claim language can broadly and reasonably be interpreted either way. Regarding the limitation "regardless of said... scoreboard bit...", since the instruction will never enter the execution stage until the predicate bit shows that the data is available, it is not used and therefore disregarded in the execute stage as claimed. As applicant states, "the decision can only be made if the scoreboard bit indicates...". The claim requires the decision be regardless of scoreboard, not the decision to make a decision. The scoreboard must update in response to nullifying an instruction. If it did not update, the scoreboard would show that the register was unavailable. Applicant states "claims 2 and 5 do not require this change of the scoreboard bit..." and then immediately contradicts this statement with "As taught by the application..., the scoreboard bit is set upon... a nullification of that write".. The scoreboard is updated in the application whether or not the nullification is done early. Regarding the additional arguments covered above, see above. Regarding the scheduling of instructions, it is performed at compile time which occurs before instructions are executed and therefore "before an instruction decode pipeline phase".. Claim 7 recites "scheduling via a complier... before an instruction decode pipeline phase". If Applicant desires to make the limitation less broad, Examiner suggest amending the claim to do so. As for the 3 signals not being obvious, events occur responsive to all 3 signals. The signals must exist or nothing could happen responsive to them. Clearly, creating signals based on events is not novel.